REMARKS

This is intended as a full and complete response to the Office Action dated July 14, 2005, having a shortened statutory period for response set to expire on October 14, 2005. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-6, 12-17, 19-24 and 29-38 are pending in the application. Claims 1-6, 12-17, 19-24 and 29-38 remain pending following entry of this response. Claims 15-16, 19, and 34-36 have been amended. The claims have been amended for clarification. Because the claims are amended for clarification and not to overcome a substantive rejection, Applicants submit that the amended claims are entitled to a full range of equivalents. Applicants submit that the amendments do not introduce new matter.

Claim Objections

Claims 15, 16 and 34 are objected to because of informalities. The claims have been amended for clarification. Applicants submit that the amended claims correct the informalities. Withdrawal of the objections is respectfully requested.

Claim Rejections - 35 U.S.C. § 101

Claims 19, 35, and 36 are rejected under 35 U.S.C. 101. Applicants respectfully submit that the rejection of claims 19, 35, and 36 is moot in light of the clarifying amendments described above. Withdrawal of the rejections is respectfully requested.

Claim Rejections - 35 U.S.C. § 102

Claims 1-6, 12-17, 19-24, 29, 34, and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by *Harper* (US. Patent 6,675,316). Applicants respectfully traverse this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as

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is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). In this case, as described below, *Harper* does not disclose "each and every element as set forth in the claim".

For example, with respect to claims 1, 12, and 29, *Harper* does not disclose executing, by a processor, a cache purge instruction that configures the processor to purge a cache line from the processor and send the cache line to at least one of a plurality of processors in the shared memory multiple processor computer system to update the at least one of a plurality of processors. The Examiner argues that *Harper* discloses the claimed element at Col. 4, lines 18-30. However, the cited passage is in fact directed to specialized circuitry called a "Flush Engine" for flushing Modified or Exclusive L2 and L3 cache lines from a node to another node. *See* Col. 4, Lines 18-30.

Harper describes a way to recover a failed computer processor having a large state size. *See* Col. 2, Lines 5-7. When a CPU node fails (*e.g.,* from a software fault or other failure), an external recovery agent is used to access memory locked in an L3 and L2 cache and force the memory out to a memory node. *See* Col. 6, Lines 10-27. The faulted node may detect its own failure using a non-maskable interrupt, panic, or other indicator. *See* Col. 7, Lines 35-39. The faulted node may either flush its own cache as part of the failure shutdown procedure or use a flush engine to traverse an L3 directory and flush every line from the L3 cache that is marked exclusive. *See* Col. 7, Lines 35-39; Col. 8, Lines 15-22. Accordingly, as described in *Harper*, flushing is performed in hardware (utilizing special circuitry, *e.g.,* the local flush engine), without the use of an instruction executed by the node. *See* Col. 4, Lines 18-30; Col. 7, Lines 35-39; Col. 8, Lines 15-22. Accordingly, Applicants respectfully submit that *Harper* does not describe executing, by a processor, a cache purge instruction that configures the processor to purge a cache line from the processor and send the cache line to at least one of a plurality of processors in the shared memory multiple processor computer system to update the at least one of a plurality of processors. Withdrawal of the rejection is respectfully requested.

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With respect to claims 29 and 35, the claims also describe executing a cache purge instruction that configures a processor to purge a cache line from the processor and send the cache line to at least one of a plurality of processors in a shared memory multiple processor computer system to update the at least one of a plurality of processors. Applicants submit that the rejection of claims 29 and 35 is overcome for at least the reasons described above. Accordingly, withdrawal of the rejection is respectfully requested.

With respect to claim 34, the claim describes a processor, which when executing a cache purge instruction is configured to purge a cache line from the processor executing the cache purge instruction and send the cache line to at least one other processor in the computer system to update at least one other processor. Again, Applicants respectfully submit that the rejection of claim 34 is overcome for at least the reasons described above. Accordingly, withdrawal of the rejection is respectfully requested.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Allowable Subject Matter

Applicants acknowledge that claims 30-33 are allowed.

Conclusion

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, Applicants believe that a detailed discussion of the secondary references is not necessary for a full and complete response to this office action.

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Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,

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